

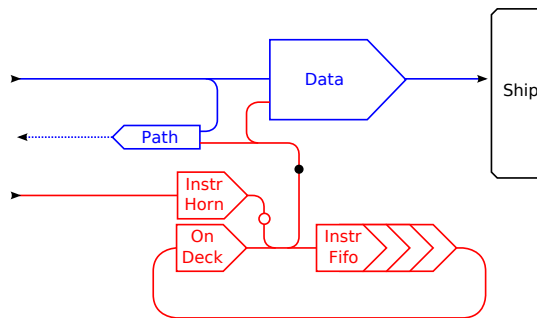
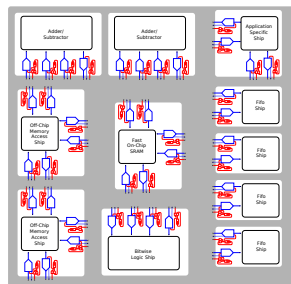
# The FleetTwo Dock

March 12, 2008

## Abstract

### Changes:

- 12-Mar renamed loop+repeat to outer+inner (not in red)
- renamed Z flag to L flag (not in red)
- rewrote "inner and outer loops" section
- updated all diagrams
- 7-Mar Moved address bits to the LSB-side of a 37-bit instruction
- Added *micro-instruction* and *composite instruction* terms
- Removed the DL field, added decrement mode to loop
- Created the Hold field
- Changed how ReLooping works
- Removed clog, unclog, interrupt, and massacre



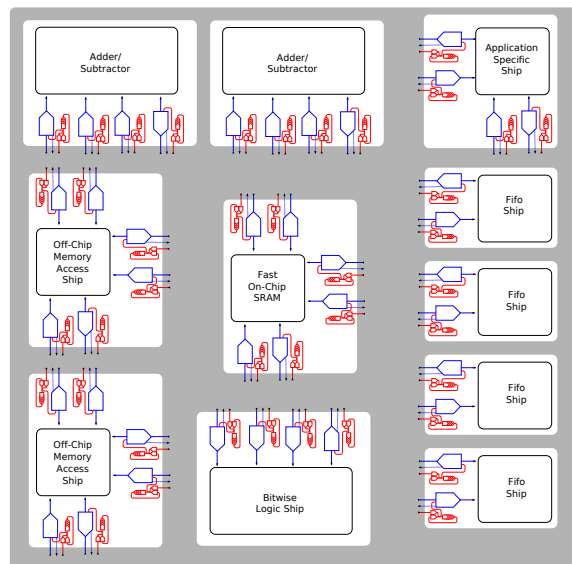
## 1 Overview of Fleet

A Fleet processor consists of a *switch fabric* with several functional units called *ships* connected to it. At each connection between a ship and the switch fabric lies a programmable element known as the *dock*.

A *path* specifies a route through the switch fabric from a particular *source* to a particular *destination*. The combination of a path and a single word *payload* is called a *packet*. The switch fabric carries packets from their sources to their destinations. Each dock has two destinations: one for *instructions* and one for *data*. A Fleet is programmed by depositing packets into the switch fabric; these packets' paths lead them to the instruction destinations of the docks.

When a packet arrives at the instruction destination of a dock, it is enqueued for execution. Before the instruction executes, it may cause the dock to wait for a packet to arrive at the dock's data destination or for a value to be presented by the ship. It may present a data value to the ship or transmit it for transmission to some other destination.

When an instruction sends a packet into the switch fabric, it may specify that the payload of the packet is irrelevant. Such packets are known as *tokens*, and consume less energy than data packets. From a programmer's perspective, a token packet is indistinguishable from a data packet with a unknown payload.



*Overview of a Fleet processor; gray shading represents a packet-switched network fabric; blue lines carry data, red lines carry instructions.*

## 2 The FleetTwo Pump

The diagram below represents a *programmer's* conceptual view of the interface between ships and the switch fabric. Actual implementation circuitry may differ substantially. Sources and destinations that can send and receive only tokens – not data items – are drawn as dashed lines.



The term *port* refers to an interface to the ship, the *dock* connecting it to the switch fabric, and the corresponding sources and destinations on the switch fabric.

Each dock consists of a *data latch*, which is as wide as a single machine word and a *pump*, which is a circular fifo of instruction-width latches. The values in the pump control the data latch.

Note that the pump in each dock has a destination of its own; this is the *instruction destination* mentioned in the previous section. Note that unlike all other destinations, there is no buffering fifo guarding this one. The size of these fifos are exposed to the software programmer so he can avoid deadlock.

### 3 Instructions

In order to cause an instruction to execute, the programmer must first cause that instruction word to arrive in the data latch of some output dock. For example, this might be the “data read” output dock of the memory access ship or the output of a fifo ship. Once an instruction has arrived at this output dock, it is *dispatched* by sending it to the *instruction port* of the dock at which it is to execute.

Each instruction is 26 bits long, which makes it possible for an instruction and an 11-bit path to fit in a single word of memory. This path is the path from the *dispatching* dock to the *executing* dock.



**Note:** the instruction encodings below are simply “something to shoot at” and a sanity check to make sure we haven’t overrun our bit budget. The final instruction encodings will probably be different.

All instruction words have the following format:



Each instruction word is called a *micro instruction*. Collections of one or more micro instruction are known as *composite instructions*.

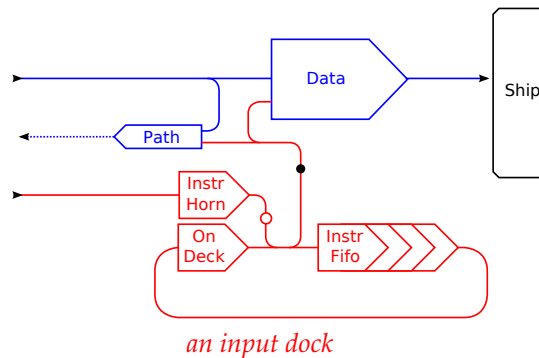
The A bit stands for *Armor*<sup>1</sup>. The OL bit indicates whether or not this instruction is part of an outer loop. Both of the preceding bits are explained in the next section.

The abbreviation P stands for *predicate*; this is a two-bit code that indicates if the instruction should be executed or ignored.

<sup>1</sup>this is to be pronounced with a Boston accent (“AAHH-mir”)

### 3.1 Life Cycle of an Instruction

The diagram below shows an input dock for purposes of illustration (behavior at an output dock is identical).



Note the circle on the path between “instr horn” and “instr fifo”; this is known as “the hatch”. The hatch has two states: sealed and unsealed. When the machine powers up, the hatch is unsealed; it is sealed by the tail instruction and unsealed as described below.

When a non-torpedo instruction arrives at the instruction horn, it waits there until the hatch is in the unsealed state. The instruction then enters the instruction fifo.

When an instruction emerges from the instruction fifo, it arrives at the “on deck” stage and starts two processes *concurrently*:

- **Process #1**  
If the instruction has the 0L bit set and the value of 0C is nonzero, this process will wait for the hatch to be *sealed* and then enqueue a duplicate copy of the instruction into the instruction fifo.
- **Process #2**  
If the value of 0C is zero and the instruction at on-deck is *not* an setOuter instruction whose 0L bit is cleared, this process will unseal the hatch, set the *inner* loop counter to zero, and terminate.

Otherwise, the instruction will execute one or more times, as determined by the flags, predicate, and inner loop counter (see below). If the instruction’s Armor bit is not set<sup>2</sup>, each execution attempt will be arbitrated against the arrival of a torpedo instruction at the instruction horn. If the torpedo wins, the *outer* loop counter is set to zero and this process terminates immediately.

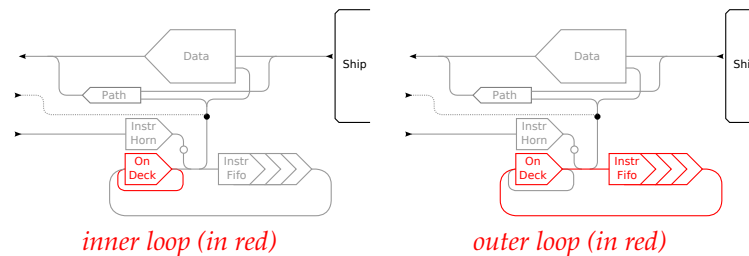
When both processes have completed, the on deck stage is vacated and another instruction may enter it.

<sup>2</sup>note: we need to say something about only send instructions being torpedoable

Note that when a torpedo arrives at the instruction horn it will wait there until on deck is occupied by an instruction whose Armor bit is *not set*, but it does *not* wait for the hatch to be unsealed.

### 3.2 Inner and Outer Loops

Using the mechanisms described above, a programmer can perform two types of loops: *inner* loops of only one instruction and *outer* loops of multiple instructions. Inner loops may be nested within an outer loop, but no other nesting of loops is allowed. The paths used by inner loops and outer loops are shown below:



Each type of loop has a counter associated with it: the IC counter for inner loops and the OC counter for outer loops. The inner loop counter applies only to send instructions; all other instructions ignore the inner loop counter. When a send instruction reaches the on deck position, it will execute at least once; the number of times it executes after that is determined by the inner loop counter.

The outer loop counter applies to all instructions *except* the instruction `setOuter` with `OL=0`, because such instructions are needed to reset the outer loop counter after it becomes zero. However, `setOuter` with `OL` set to *one* is useful for resetting the loop counter in the middle of the execution of a loop.

### 3.3 Flags

The pump has four flags: A, B, S, L. Of these four, only the first two may be modified directly by instructions.

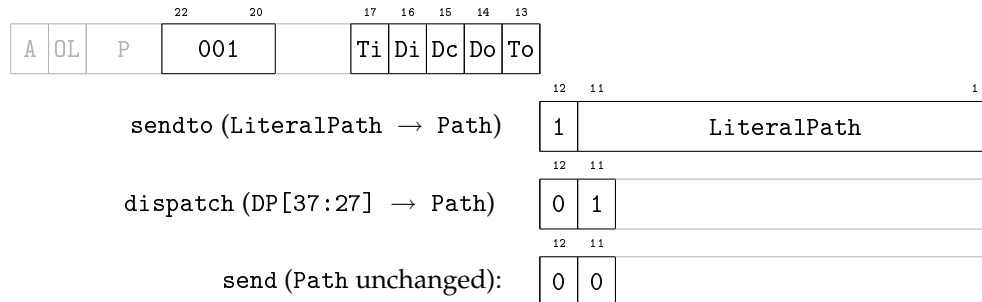
- The A and B flags are general-purpose flags which may be set and cleared by the programmer.
- The L flag, known as the *last flag*, is set whenever the value in the outer counter (OC) is one, indicating that the dock is in the midst of the last iteration of an outer loop. This flag can be used to perform certain operations (such as sending a completion token) only on the last iteration of an outer loop.

- The S flag, known as the *summary* flag. Its value is determined by the ship, but unless stated otherwise, it should be assumed that whenever the 37th bit of the data (D) latch is loaded, that same bit is also loaded into the S flag. This lets the ship make decisions based on whether or not the top bit of the data latch is set; if two's complement numbers are in use, this will indicate whether or not the latched value is negative.

Many instruction fields are specified as two-bit *predicates*. These fields contain one of four values, indicating if an action should be taken unconditionally or conditionally on one of the A or B flags:

- 00: if A is set
- 10: if B is set
- 01: if L is set (OC=1)
- 11: always

## 3.4 send (variants: sendto, dispatch)



- Ti - Token Input: wait for the token predecessor to be full and drain it.
- Di - Data Input: wait for the data predecessor to be full and drain it.
- Dc - Data Capture: pulse the data latch.
- Do - Data Output: fill the data successor.
- To - Token Output: fill the token successor.

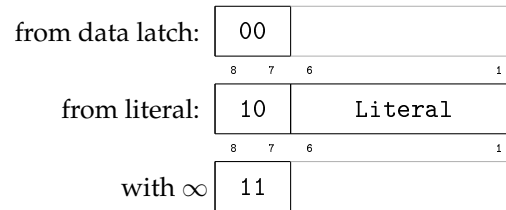
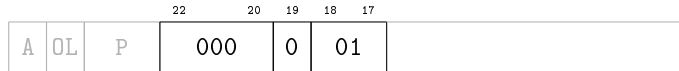
The data successor and token successor must both be empty in order for a send instruction to attempt execution.

The inner loop counter can hold a number  $0..MAX$  or a special value  $\infty$ . If IC is nonzero after execution of a send instruction, the instruction will execute again, and IC will be latched with  $(IC = \infty ? \infty : \max(IC - 1, 0))$ . When the inner loop counter reaches zero, the instruction ceases executing.



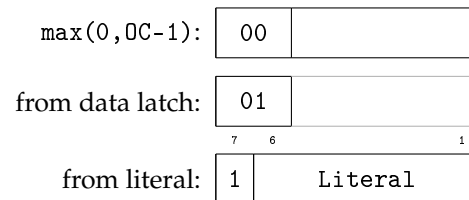
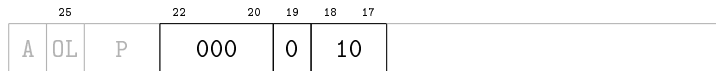
## 3.7 setInner

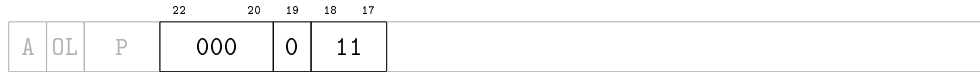
This instruction loads the inner loop counter with either a literal number, the special value  $\infty$ , or the contents of the data register.



## 3.8 setOuter

This instruction loads the outer loop counter OC with either  $\max(0, OC-1)$ , a literal or the contents of the data register.



**3.9 takeOuterLoopCounter**

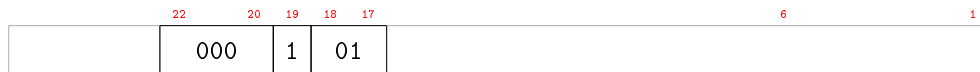
This instruction copies the value in the outer loop counter OC into the least significant bits of the data latch and leaves all other bits of the data latch unchanged.

**3.10 takeInnerLoopCounter**

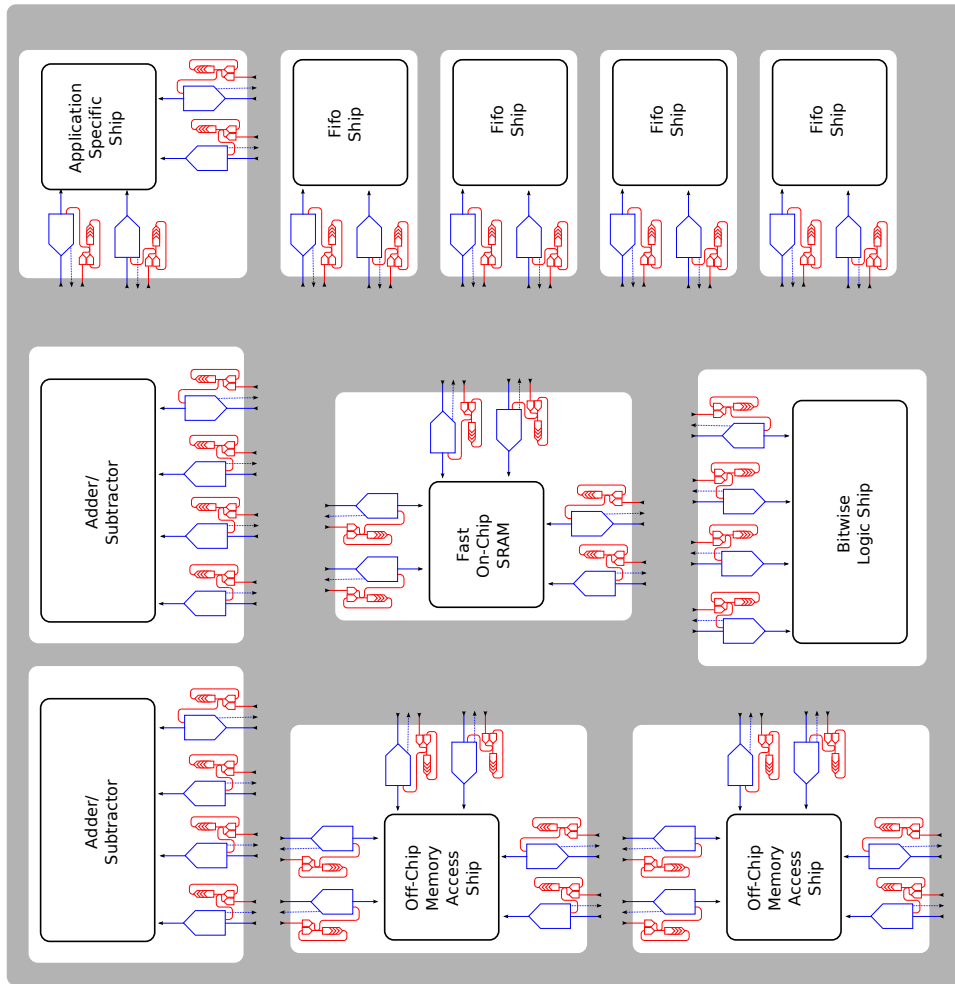
This instruction copies the value in the inner loop counter IC into the least significant bits of the data latch and leaves all other bits of the data latch unchanged.

**3.11 torpedo**

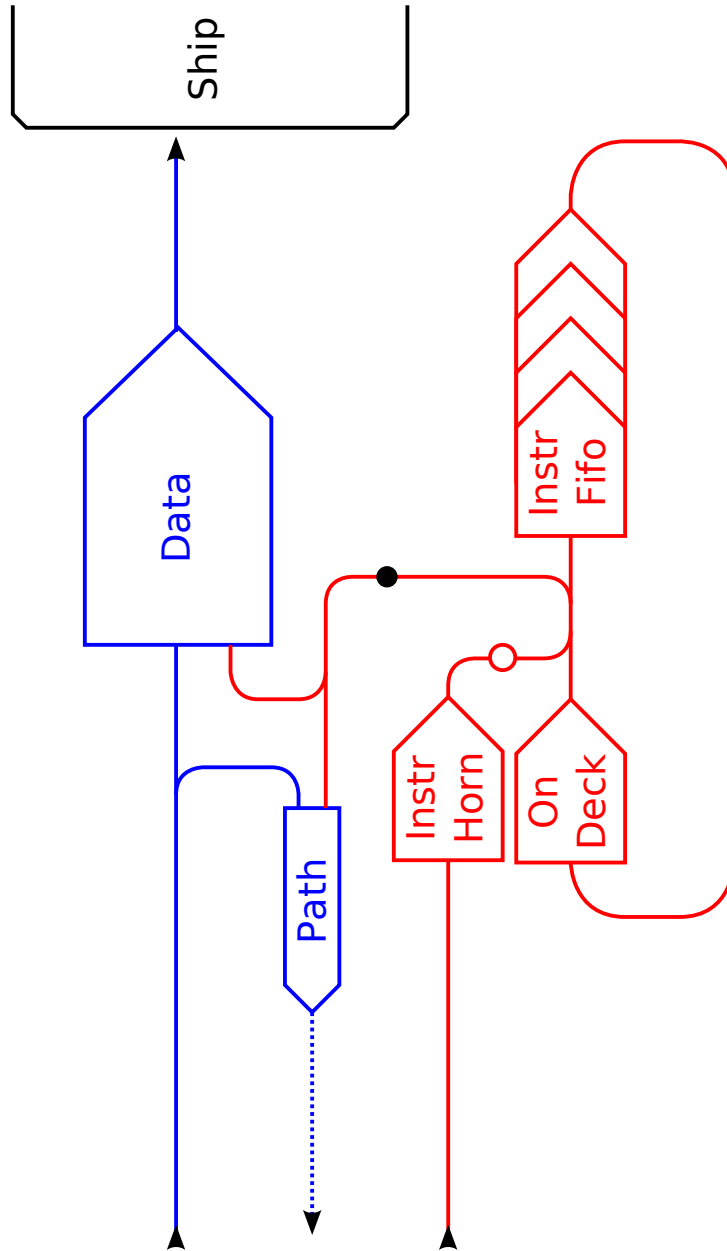
When a torpedo instruction reaches the instruction horn, it will wait there until an instruction is on deck whose Armor bit is not set. The torpedo will then cause "Process #2" of the on deck instruction to terminate and will set the outer loop counter to zero.

**3.12 tail**

When a tail instruction reaches IH, it seals the hatch. The tail instruction does not enter the instruction fifo.



## Input Dock



Output Dock

