

UC Berkeley Computer Science

Subject: Results of a Design Review of Infinity
Date: May 17, 2007
From: Ivan Sutherland and Ian Jones
UCIES #2007-is48

References:

UCIES #2007-is46 Infinity: A Proposed Test Chip, Ivan Sutherland, 18 April 2007
UCIES #2007-is47: An Outline for the Review of Infinity, Ivan Sutherland, 13 May 2007
An almost identical version of this memo, for internal Sun use only, is called SML# 2007-0225. I have expunged a few references to internal Sun documents from this version.

PURPOSE

This memo attempts to record the suggestions made during the 15 May design review of Infinity. The text of this memo expands on notes made by Ian Jones; a scan of the notes is attached. The order of suggestions in this memo conforms with that of Ian's notes, which were taken as the review progressed.

The suggestions fit into three categories: reliability, performance, and capability. Suggestions for improved reliability are of most importance. We must make these suggested changes. Suggestions that improve performance are valuable but not essential. We'll make such changes if possible. Finally, suggestions for greater capacity are most welcome. With them, we may obtain greater value from the chip.

1, 7) ARBITER – basicGasP-C (performance)

The final pull-up on the arbiter adds capacitance to the mutual exclusion flip flop. One might use a pseudo N-MOS circuit to reduce this capacitance. A passive pull-up adds less capacitance to the mutual exclusion element.

The Arbiter might better be split into two or more stages for better logical effort. This matches my intuition, but I can't see how to do it.

2) UNKEPT STATE-WIRE – basicGasP-F (reliability)

The conditional successor driver in a branch turns off the keeper to both successor state wires when either is driven. This is just when there's most likely to be noise. A better design would retain the keeping action on any state wire that's not about to be driven. The address bit itself can serve this purpose.

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3) SEPARATE DRIVE FOR Address[1] and the “T” bit – (reliability?)

One might give special early treatment to the two bits with critical timing. Because there are only two, they might be driven a whole gate delay earlier with small load penalty. This idea is worth careful thought if the timing is anywhere near critical.

4-5) BEWARE TRANSISTOR VARIABILITY – basicGasP-J (reliability)

The self-resetting amplifiers that drive the latches need simulation with transistor variability taken into account. It's possible, for example, that strong N and weak P transistors might damage the timing. Both “corner” cases and “statistical” variability need study.

6) LOCATION OF SELF-RESET SIGNALS (performance)

One might wish to take the self-reset signals from part way down the latch drive wires to be sure the latch wires are properly driven.

8) LATCHES (reliability)

Data input to the latches should drive transistor gates rather than pass gate diffusion. That offers better noise immunity because a pass gate may conduct when it's not supposed to if noise drives its input beyond the rails.

Separate the feedback inverter in the latch from the output drive for better noise immunity on the output wire.

9) CHARACTERIZE THE PROCESS WITH DUTCHESS (capability)

We have the Duchess ring oscillators and should put them on this chip.

10) VOLTAGE SAMPLERS (capability)

Two kinds of voltage samplers are possible. First, a wire that conveys the power and ground values from near the center of the chip to a pair of pads can let us measure the internal supply voltage.

Second, one can build onto the chip some high speed voltage samplers that would let us observe internal wave forms. We need access to the appropriate circuits.

11) FILL CELLS (reliability)

Fill cells outside the area of the experiment need to include bypass capacitance. Fill cells over the experiment need to include power delivery. How will we provide suitable fill cells? Pitch matching is the problem.

My initial plan is to use Java code to generate the fill. But how will that accommodate the pads and experiments not included in the Java data base?

12) CHIP SIMULATION (testing)

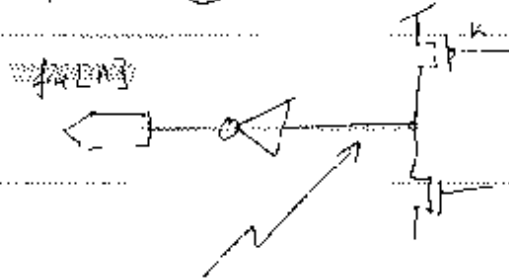
We need test code for Infinity. We can run that test code on the circuits prior to making the chip. I plan to ask Amir, summer intern, to undertake this task.

13) FAILURE TO TEST THE CROSS STAGE (capability)

Nowhere does Infinity test the Cross stage. It could easily be tested by counting the number of elements that pass through various parallel paths connected by branch, merge, and cross. The idea of using a count (which hadn't occurred to me) makes such a test practical. We could put such a pattern in the center column, or in a separate ring used specifically for that purpose.

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1. Sense GasP - C



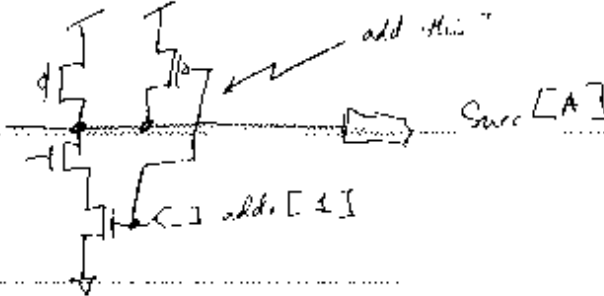
this node needs a battery keeper here on reset, to pull H

50 SHEETS
50 SHEETS
50 SHEETS

2. Sense GasP - F

use addr bit to keep keepers on for unreset state wire

eg:



3. Separate paths (lower logical effort)

to deliver the "T" and "addr [1]" bits
- critical timing paths

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o Careful tuning issues for

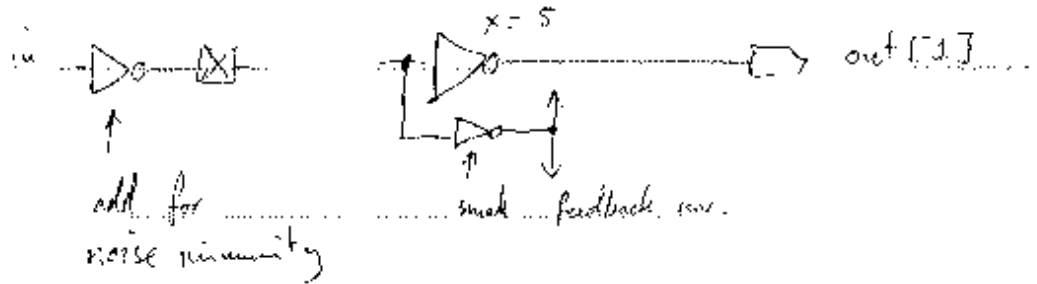
3-gate delay pulses
with long wires

transistor to transistor variations are large;

50 SHEETS
100 SHEETS
150 SHEETS
200 SHEETS5. "Corner" & "Statistical" simulation
to try to catch the best cases6. Pick self-reset signal from
some way down the width of the data
latches rather than from the drive point.7. pseudo-NMOS pull-ups in arbiters?

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8. HI 2in Latch



9. Put "Dutchess" on the chip?

10. Add voltage samples to help determine timing margin of T-bit?

11. Metal-fill cells

12. Intend to do 5-bit emulation of \log_2 thing

13. Branch in center to use X stages